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EXAMINER	
DESTA, ELIAS	

ART UNIT	PAPER NUMBER
2857	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/566,461	MATTES ET AL.	
	Examiner	Art Unit	
	Elias Desta	2857	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 September 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *21-44* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *21,22,25,27-30,35-41 and 44* is/are rejected.

7)☒ Claim(s) *23, 24,26, 31-34, 42 and 43* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 January 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *1/30/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Detailed Action

Claim Objection

1. Claims 33 and 34 are objected to because of the following minor informalities: claim 33, seven lines from the end of the claim does not have a linking operator: "... by the reference signal generator by the signal generators..." appropriate change is required. Claim 34 is objected to because of its dependency on the objected base claim 33.

Claim rejection – 35 U.S.C. 101

2. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

3. Claims 35-40 are directed to non-statutory subject matter because: in reference to claim 35: the claim includes two statutory categories, namely method and apparatus in the same claim. Applicant is required to make a distinction between the two categories: in reference to claims 36-40: claim 36 is a computer program per se, therefore, claim 36 by itself should fulfill the statutory requirement or the guideline for computer programs. In other words, the program structure in claim 36 has to be contained or reside in a memory and should be executable in order to meet the statutory requirement. Claims 37-40 are also rejected to the extent that they inherit the elements of the base claim 36.

Claim rejection – 35 U.S.C. 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 21, 25, 28-30 and 44 are rejected under 35 U.S.C. 103 (a) as being unpatentable over *Folkesson et al.* (IEEE Article, 'Modeling of Dynamic Errors in Algorithmic A/D converters', hereon *Folkesson*) in view of *Fan et al.* (U.S. Patent 6,703,885, hereon *Fan*).

In reference to claims 21, 25 and 44: *Folkesson* teaches a test device for testing circuits (such as A/D converter) (see *Folkesson*, page 455, Introduction). The test arrangement comprises:

- A precision signal generator, configured for generating a test signal and coupled to an input contact for coupling to an input of an integrated circuit (see *Folkesson*, page 457, section 5, 'Measurements and simulations');
- A reference signal generator configured for generating a reference signal (see *Folkesson*, page 455, Fig. 1);
- A comparator unit (see *Folkesson*, page 455, Fig. 2).

However, *Folkesson* does not fully teach a comparator for input contact, the comparable being operable in a test mode and being configured such that the test signal is compared with the

reference signal and that the comparator can turn off the precision signal generator if the test signal exceeds or falls below the reference signal.

Fan teaches a trimmer device where a reference signal of a target circuit (precision signal generator) is compared with a test signal, and a binary count output is generated according to result of a comparison, the counter coupled to the switch device and operable so as to generate a binary count output that is used to selectively turn on or turn off the transistor units of the switch device (see *Fan*, column 2, lines 61-67).

Therefore, it would have been obvious at the time the invention was made to a person having ordinary skill in the art to modify the comparator circuit as taught by *Folkesson* in order to operate the comparator in a test mode (as noted in Fan) where the precision signal generator (target circuit) can be turned off by the comparator unit if the test signal exceeds or falls below the reference signal because by operating the comparator in a test mode enables the system to minimize noise reception and set the reference signal to be approximate to the test signal (see *Fan*, column 2, lines 26-28 and column 3, lines 10-11) as a result the testing provides a better production testing and efficiency (see *Fan*, column 1, lines 12-19).

With regard to claim 27: *Folkesson* in combination Fan further teaches that the test device includes a decision logic unit coupled to the comparator unit and which is configured such that control signals are generated for the precision signal generator from the output signals of the comparator unit (see *Folkesson*, Fig. 1, Principle of the ADC, further the combination is illustrated in *Fan*, column 2, line 65 to column 2, line 11).

With regard to claim 28: *Folkesson* further teaches that a respective output contact for coupling to an output of an integrated circuit (ADC) is provided for each input contact, the output contact being coupled to an output line (see *Folkesson*, Figs. 1 and 2).

With regard to claim 29: *Folkesson* further teaches that the validation signal line leads from the comparator unit to the relevant output line (*Folkesson*, page 455, Fig. 2).

With regard to claim 30: *Folkesson* further teaches that the test device is integrated with the integrated circuit or ADC because the system uses a successive approximation architecture where the system includes the ADC model with comparator block units (see *Folkesson*, page 455, Figs. 1, 2 and sections 1 & 2).

6. Claims 22 and 41 are rejected under 35 U.S.C. 103(a) as being unpatentable over *Folkesson et al.* (IEEE Article, 'Modeling of Dynamic Errors in Algorithmic A/D converters', hereon *Folkesson*) and *Fan et al.* (U.S. Patent 6,703,885, hereon *Fan*) in view of *Noda* (U.S. Patent 5,870,042).

In reference to claim 22: *Folkesson* teaches a test device for testing circuits (such as A/D converter) (see *Folkesson*, page 455, Introduction). However, *Folkesson* does not teach a test device having two reference signal generators where the first reference signal generator configured for generating a lower reference signal and a second reference signal generator configured for generating an upper reference signal, a first comparator unit, which is connectable to the first reference signal generator, and a second comparator unit, which is connectable to the second reference signal generator, being provided for each input contact.

Noda teaches a test device comprises two reference signal generators where the first reference signal generator is configured for generating a lower reference signal (see *Noda*, Fig. 7, SP 11) and a second reference signal generator configured for generating an upper reference signal (see Fig. 7, SP 9), a first comparator unit, which is connectable to the first reference signal generator, a second comparator unit, which is connectable to the second reference signal generator, being provided for each input contact (see *Noda*, Fig. 2 and column 3, lines 60-67).

Therefore, it would have been obvious at the time the invention was made to a person having ordinary skill in the art to modify test device for testing circuits (such as A/D converter) as taught by *Folkesson* and incorporate two reference signal generators where the first reference signal generator is configured for generating a lower reference signal (see *Noda*, Fig. 7, SP 11) and a second reference signal generator configured for generating an upper reference signal (see Fig. 7, SP 9) with their respective comparator units because the modification would provide the user to obtain a linear ideal A/D conversion and enables the system to obtain a current waveform corresponding to the ideal A/D conversion characteristic (see *Noda*, column 4, lines 2-6 and 14-24).

In reference to claim 41: *Folkesson* teaches a test device for testing circuits (such as A/D converter) (see *Folkesson*, page 455, Introduction). The test arrangement comprises:

- A precision signal generator, configured for generating a test signal and coupled to an input contact for coupling to an input of an integrated circuit (see *Folkesson*, page 457, section 5, 'Measurements and simulations');

- A reference signal generator configured for generating a reference signal (see *Folkesson*, page 455, Fig. 1); and
- A comparator unit (see *Folkesson*, page 455, Fig. 2).

However, *Folkesson* does not fully teach a comparator for input contact, the comparable being operable in a test mode and being configured such that the test signal is compared with the reference signal and that the comparator can turn off the precision signal generator if the test signal exceeds or falls below the reference signal.

Fan teaches a trimmer device where a reference signal of a target circuit (precision signal generator) is compared with a test signal, and a binary count output is generated according to result of a comparison, the counter coupled to the switch device and operable so as to generate a binary count output that is used to selectively turn on or turn off the transistor units of the switch device (see *Fan*, column 2, lines 61-67).

Therefore, it would have been obvious at the time the invention was made to a person having ordinary skill in the art to modify the comparator circuit as taught by *Folkesson* in order to operate the comparator in a test mode (as noted in Fan) where the precision signal generator (target circuit) can be turned off by the comparator unit if the test signal exceeds or falls below the reference signal because by operating the comparator in a test mode enables the system to minimize noise reception and set the reference signal to be approximate to the test signal (see *Fan*, column 2, lines 26-28 and column 3, lines 10-11) as a result the testing provides a better production testing and efficiency (see *Fan*, column 1, lines 12-19).

Further, *Folkesson* does not teach a test device having two reference signal generators where the first reference signal generator configured for generating a lower reference signal and a second reference signal generator configured for generating an upper reference signal, a first comparator unit, which is connectable to the first reference signal generator, and a second comparator unit, which is connectable to the second reference signal generator, being provided for each input contact.

Noda teaches a test device comprises two reference signal generators where the first reference signal generator is configured for generating a lower reference signal (see *Noda*, Fig. 7, SP 11) and a second reference signal generator configured for generating an upper reference signal (see Fig. 7, SP 9), a first comparator unit, which is connectable to the first reference signal generator, a second comparator unit, which is connectable to the second reference signal generator, being provided for each input contact (see *Noda*, Fig. 2 and column 3, lines 60-67).

Therefore, it would have been obvious at the time the invention was made to a person having ordinary skill in the art to modify test device for testing circuits (such as A/D converter) as taught by *Folkesson* and incorporate two reference signal generators where the first reference signal generator is configured for generating a lower reference signal (see *Noda*, Fig. 7, SP 11) and a second reference signal generator configured for generating an upper reference signal (see Fig. 7, SP 9) with their respective comparator units because the modification would provide the user to obtain a linear ideal A/D conversion and enables the system to obtain a current waveform corresponding to the ideal A/D conversion characteristic (see *Noda*, column 4, lines 2-6 and 14-24).

Allowable Subject Matter

7. Claims 23, 24, 26, 27, 31, 42 and 43 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

In reference to claim 23: *Folkesson* or *Noda* does not teach a test device having a reference signal generator which has "a calibration line and reference line, the comparator unit being connected to the calibration line and to the reference line of the reference signal generator, comparator unit having calibration unit, and the comparator unit also being operable in a calibration mode configured such that the switching properties of the comparator unit are adjustable by the calibration unit by means of the signal values of the calibration line which are present at the comparator unit and by mans of the reference line."

With regard to claim 26: *Folkesson* or *Noda* does not teach a test device having the "comparator having two inputs and an output, the first input of the comparator being coupled the reference line of the reference signal generator, the second input of the comparator being coupled to the calibration line of the reference signal generator and the connecting line of its input contact, the output of the comparator being coupled to the calibration unit and to the precession signal generator and the switching properties of the calibration unit being adjustable by the comparator.

With regard to claim 27: *Folkesson* or *Noda* does not teach a test device having "a decision logic unit [which] is coupled to the comparator unit and which is [also] configured such

that control signals are generated for the precision signal generator from the output signals of the comparator unit."

With regard to claim 31: *Folkesson* or *Noda* does not teach a test device having "a load board for receiving at least one needle card for testing integrated circuits and having at least one test receptacle for testing integrated circuits and for connecting a handler to a tester of integrated circuits, the load board having a test device," and claim 32 further adds the limitation the test device having "...a precision signal generator and the reference signal generator being formed on the tester, and the comparator unit with the calibration unit being arranged on the load board, adjacent to the input contacts for the integrated circuit."

With regard to claim 42: *Folkesson* or *Noda* does not teach a test device having first and second signal generator each having a calibration line and a reference line, each comparator unit being connected to the calibration line and to the reference line of the relevant reference signal generator, each comparator unit having a calibration unit, and the comparator unit also being operable in calibration mode configured such that the switching properties of the comparator unit are adjustable by the calibration unit by means of the signal values of the calibration line which are present at the comparator unit and by means of the reference line."

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant disclosure:

a. *Ebihara* (U.S. Patent 5,107,205) teaches semiconductor device tester with a test waveform monitoring circuit.

b. *Williams* (U.S. Patent 6,344,749) teaches test system for measuring frequency response and dynamic range on cable plant.

c. *Sakaguchi* (U.S. Patent 6,766,266) teaches testing device and testing method for semiconductor integrated circuits.

d. *Roberts et al.* (U.S. Patent 6,931,579) teaches integrated excitation/extraction system for test and measurement.

e. *Callahan, Jr.* (U.S. Patent 6,586,980) teaches driver circuit having a slew rate control system with improved linear ramp generation including ground.

f. *Faulk et al.* (U.S. Patent 5,768,118) teaches a power converter which transfers energy from an output circuit coupled to a secondary winding of a power transformer to an output circuit in order to reduce EMI effect.

g. *Hock* (U.S. Patent 4,238,695) teaches comparator circuit having high speed and high current switching capability.

h. *Niiyama et al.* (U.S. PAP 2005/0007089) teaches step-up/step-down DC-DC converter and portable device employing the converter.

i. *Ren* (IEEE Article, 'A High Precision On-Site Measurement Calibration Device for Heavy Direct Current') discusses the principle of operation and the characteristics of the comparator, the double-shielded design and the analysis of its error.

j. *MacGugan* (U.S. Patent 6,653,872) teaches multi-channel precision synchronous voltage-to-frequency converter.

k. *Carson* (U.S. Patent 5,424,677) teaches common mode error correction for differential amplifiers.

l. *Han et al.* (IEEE Article, 'Analogue Divider Using Integral Compare Mode and Its Application') discusses a type of analogue divider that consist of two integral operators, a comparator and two electronic switches.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Elias Desta whose telephone number is (571)-272-2214. The examiner can normally be reached on M-Fri (10:30-7:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eliseo Ramos-Feliciano can be reached on (571)-272-7925. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

10. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Elias Desta
Examiner
Art Unit 2857

- E.D.

- August 27, 2007

CAROL S.W TSAI
PRIMARY EXAMINER